

# AD33AA8P11 Gate Drive Technical Manual

## P100503

This document is suitable for use with the following Amantys gate drive which supports configuration via Power Insight.

AD33AA8P11 Off-module Single Gate Drive with 1700V or 3300V Module Interface Card

This is a customer specific part number, the board is also known as AD00XA8. Not all features are common to all Amantys gate drives. For further information, refer to *Section 2. Identifying the Gate Drive Version and Revision*. This manual is based on P100191 which covers all of the other Amantys configurable gate drives.

Refer to the product datasheet for specific voltage variants, 1700V and 3300V, as the same gate drive is used with different components fitted to the module interface card.

This document does not describe Power Insight in detail. Please refer to alternative documentation and specific gate drive datasheets for further information.

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## Important

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The information contained herein is intended exclusively for qualified engineers who are experienced with, and trained in, working with high voltage apparatus which involves risk to life. Strict compliance with all relevant safety regulations for the target application is essential.

Any handling of electronic devices is subject to the general specifications for protecting electrostatic sensitive devices according to international standard IEC 747-1, Chapter IX or European standard EN 100015 (i.e. the workplace, tool, operating environment, etc. must comply with these standards). Failure to comply may lead to the product becoming damaged.

**WARNING: High voltage equipment - for use by trained personnel only.**



Failure to observe electrical shock precautions while the equipment is in operation may result in personal injury, electrical shock damage to, or destruction of components of this equipment.

**CAUTION:** When handling the gate drive and the IGBT module, observe electro-static precautions. If these precautions are not taken, permanent damage to the components may result.



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## Technical Support

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For technical support please visit [www.amantys.com](http://www.amantys.com).

For IGBT module data refer to the manufacturer's data sheet.

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## Quality Control

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The gate drive is manufactured according to ISO9001:2000 quality standards.

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## Product Customisation

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Contact Amantys Power Electronics Ltd to discuss any product customisation requirements. Contact details can be found on the website.

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## Legal Disclaimer

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This document describes devices but cannot promise to deliver any specific characteristics. No warranty or guarantee is given - either expressly or implicitly - regarding delivery, performance or suitability.

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## 1 Introduction

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The Amantys gate drive is a high performance, single channel drive suitable for high-power IGBT modules. They are configurable and capable of driving modules from all leading IGBT manufacturers without the need to add external gate resistors and capacitors giving greater design and reuse flexibility.

This document is suitable for use with the off-module 1700V and 3300V single channel gate drive although it shares many similarities with other Amantys gate drive products.

In its simplest form a gate drive has one optical input to turn the IGBT on and off, and one optical output to acknowledge the switching edge and signal a fault. Various status and fault signalling protocols are supported. Power is provided by a pair of wires at 14V to 30V and the gate drive features an isolated DC-DC converter to provide the local supplies.

The output drive stage is a traditional voltage source with configurable turn-on, turn-off and soft-turn-off resistors. Some gate drive configurations feature an extra turn-off resistor that is selected when the DC link is above a programmed threshold. This is useful for situations where the DC link can rise for a short time (such as under low load or braking) and it prevents unnecessary stress on the clamping components.

Status LEDs are provided to facilitate identification of normal operation and fault conditions. Refer to the relevant datasheet for information about what the LEDs mean.

As Amantys products are digital gate drives, they feature a range of programmable registers and configuration options to suit a variety of target IGBT modules and applications. The user should take care not to accidentally disable the fault protection features.

Amantys gate drives have interfaces to allow programming of the complex programmable logic device (CPLD) and the micro-controller in the factory, but user updates can be made in the field over the fibre-optic interface using a Power Insight Adapter and the Power Insight Configurator software tool that runs on any Windows PC.

The gate drive is coupled to the IGBT module with additional circuitry close to the IGBT module known as a Module Interface Card (MIC) as shown in Figure 1, and a cable with high-voltage insulation.

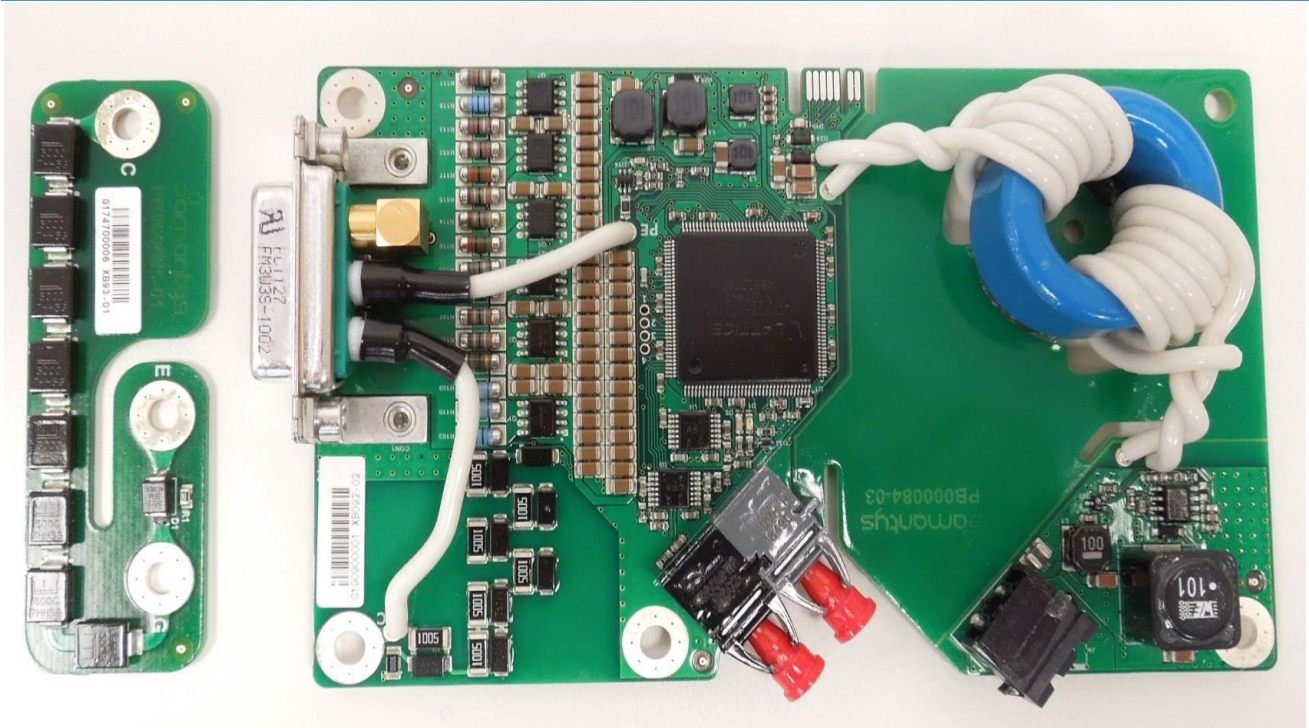


Figure 1. Off-module Gate Drive and Module Interface Card

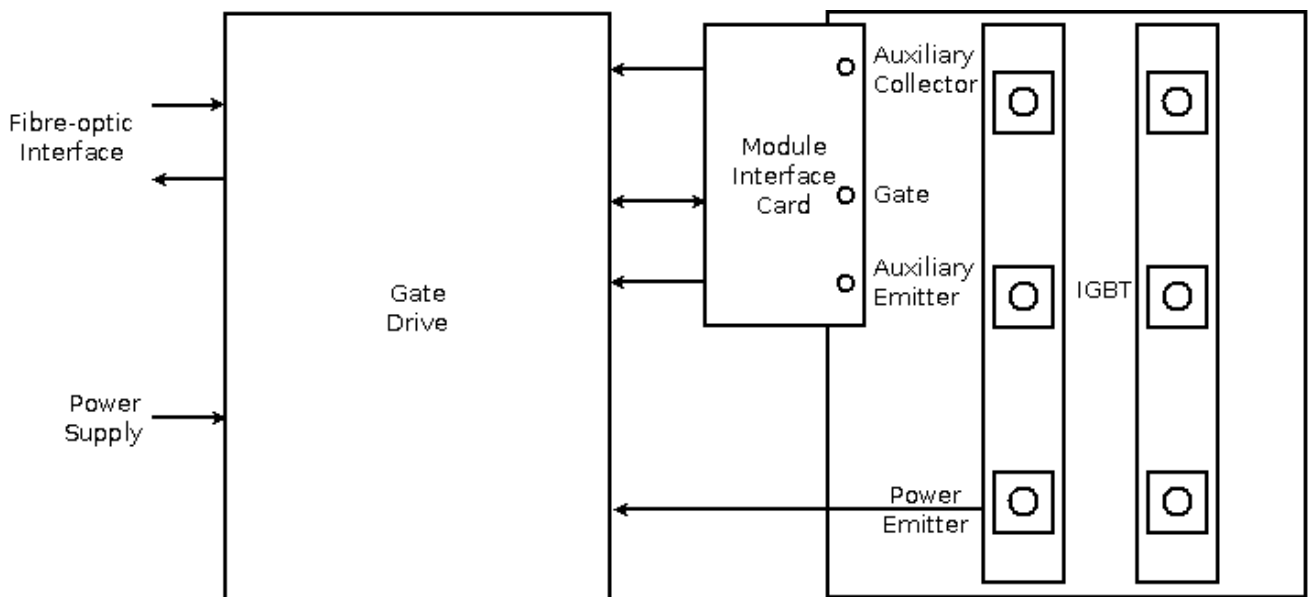


Figure 2. Block Diagram Showing Gate Drive, Connections and Module Interface Card

## 2 Identifying the Gate Drive Version and Revision

The Amantys gate drive is designed to be used with, and configured by, the [Power Insight Configurator](#). Figure 3 is a screen shot showing the Diagnostics tab for the gate drive connected to port 3 of the Power Insight Adapter. For support purposes it may be helpful to write this information to a text file using the “Save to Text File” button provided.

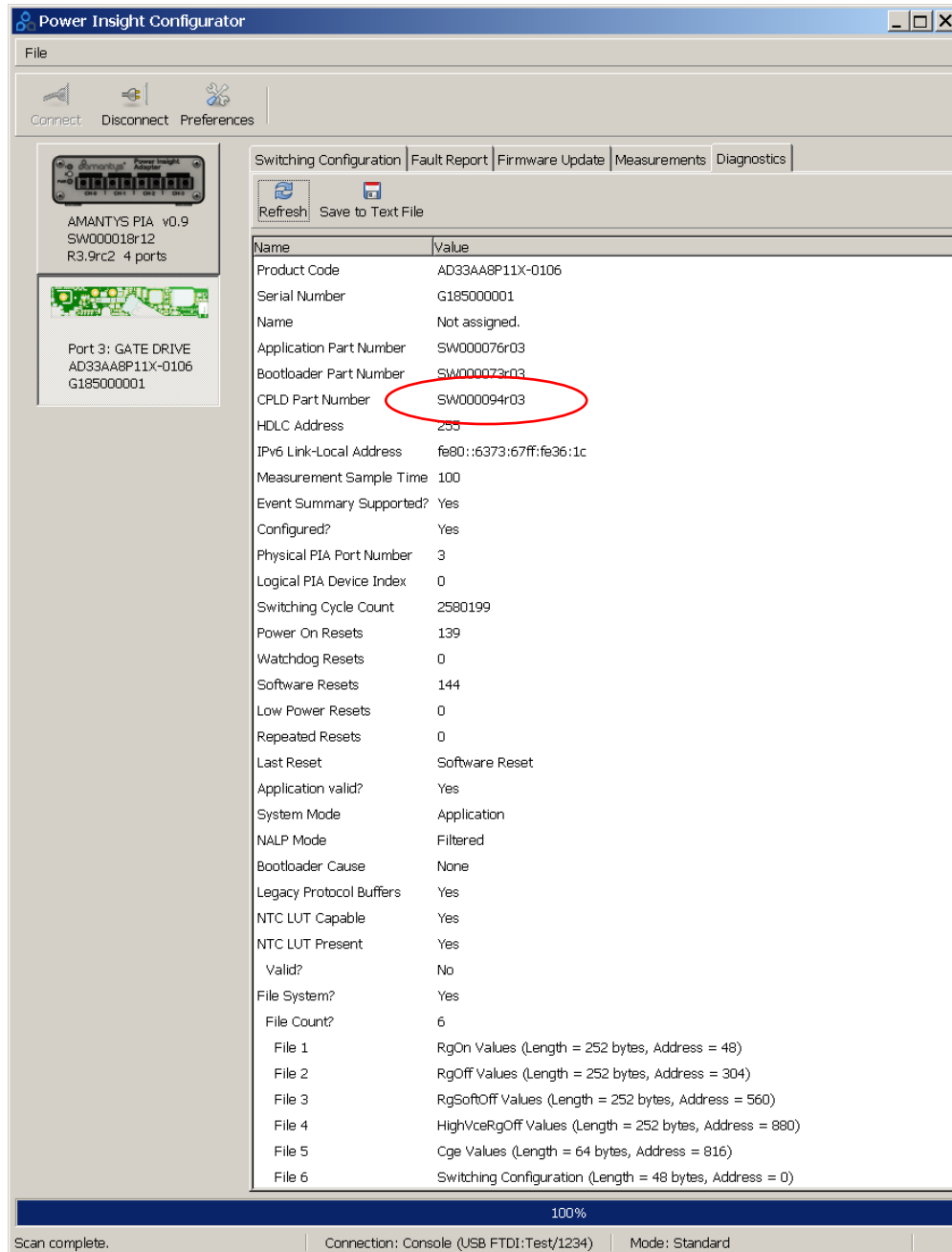


Figure 3. Screen-shot of the Power Insight Configurator, Gate Drive Diagnostics tab

To identify features of the hardware it is useful to make a note of the “CPLD Part Number” and revision which will be as shown as in Figure 3. The Configurator reads this information and from it decides which configuration parameters to show in the “Switching Configuration” tab, Figure 4.

**Power Insight Configurator**

File Help

Connect Disconnect Preferences

AMANTYS PIA v0.9  
SW000018r12  
R3.9rc2 4 ports

Port 3: GATE DRIVE  
AD33AA8P11X-0106  
G185000001

Switching Configuration | Fault Report | Firmware Update | Measurements | Diagnostics

Load from File Save to File Undo Redo Assign Name Update Data File(s) Configure NTC Extract Filesystem Write Filesystem

| Name                                   | Value      | Min     | Max       |
|--|------------|---------|-----------|
| Gate Turn On Resistor                  | 3.900 Ω    | 0.47    | 27.00     |
| Gate Turn Off Resistor                 | 3.988 Ω    | 1.02    | 56.00     |
| Gate Soft Turn Off Resistor            | 22.000 Ω   | 1.02    | 56.00     |
| DC Link Measurement Enable             | 0          | 0       | 1         |
| High Vce Gate Turn Off Resistor        | 15.795 Ω   | 1.02    | 56.00     |
| Gate-Emitter Capacitance               | 100.000 nF | 0.00    | 328.00    |
| Disable Turn-off on Fault              | 0          | 0       | 1         |
| Feedback Protocol                      | 5          | 0       | 15        |
| Fault Lock-out Time                    | 100 ms     | 0.00    | 64,000.00 |
| Desat Window Time 1                    | 5 μs       | 0.00    | 1,310.00  |
| Desat Window Time 2                    | 5 μs       | 0.00    | 1,310.00  |
| Desat Window Time 3                    | 5 μs       | 0.00    | 1,310.00  |
| Desat Window Time 4                    | 20 μs      | 0.00    | 1,310.00  |
| Gate Monitor 1 Time (ON)               | 20 μs      | 0.00    | 1,310.00  |
| Gate Monitor 2 Time (OFF)              | 20 μs      | 0.00    | 1,310.00  |
| Turn On Delay                          | 0 μs       | 0.00    | 5.00      |
| Turn Off Delay                         | 0 μs       | 0.00    | 5.00      |
| Type 2 Short Circuit to Turn Off Delay | 0 μs       | 0.00    | 5.00      |
| Vce Monitor Filter Time Constant       | 2 μs       | 0.00    | 5.00      |
| Desat Diode 1 Enable                   | 0          | 0       | 15        |
| Desat Diode 2 Enable                   | 0          | 0       | 15        |
| Vce Monitor 1 Enable                   | 0          | 0       | 15        |
| Vce Monitor 2 Enable                   | 0          | 0       | 15        |
| Vce Monitor 3 Enable                   | 0          | 0       | 15        |
| Gate Monitor 1 Enable                  | 1          | 0       | 1         |
| Gate Monitor 2 Enable                  | 0          | 0       | 1         |
| Desat Diode 1 Comparator Threshold     | 35.29 V    | 0.00    | 35.29     |
| Desat Diode 2 Comparator Threshold     | 0 V        | 0.00    | 35.29     |
| Vce Monitor 1 Comparator Threshold     | 494.59 V   | -404.00 | 3,616.00  |
| Vce Monitor 2 Comparator Threshold     | 999.06 V   | -404.00 | 3,616.00  |
| Vce Monitor 3 Comparator Threshold     | 1992.24 V  | -404.00 | 3,616.00  |
| Vce Monitor 4 Comparator Threshold     | 1992.24 V  | -404.00 | 3,616.00  |
| Gate Monitor 1 Comparator Threshold    | 10.06 V    | -15.50  | 18.80     |
| Gate Monitor 2 Comparator Threshold    | -4.07 V    | -15.50  | 18.80     |
| di/dt Monitor 1 Threshold              | 112        | 0       | 255       |
| di/dt Monitor 2 Threshold              | 120        | 0       | 255       |
| di/dt Filter 1 Time Constant           | 4 μs       | 0.00    | 5.00      |
| di/dt Filter 2 Time Constant           | 4 μs       | 0.00    | 5.00      |
| di/dt Enable 1                         | 0          | 0       | 1         |
| di/dt Enable 2                         | 0          | 0       | 1         |
| Fibre Drive Current                    | 3.64 mA    | 1.82    | 6.37      |
| High Frequency Limit Enable            | 0          | 0       | 1         |
| Minimum Pulse Width                    | 50.98 μs   | 0.00    | 1,310.00  |
| Minimum Pulse Width Fault Enable       | 1          | 0       | 1         |
| Test Config Enable                     | 0          | 0       | 1         |
| Debug                                  | 0          | 0       | 15        |

Change the parameter values by typing them directly into the table or by loading a configuration from a file. Changed parameter values will appear in red

Send the configuration to the gate drive using the buttons below

Apply Config to Gate Drive

Apply this Config to all compatible Gate Drives

Undo all changes

100%

Scanning for device changes... Connection: Console (USB FTDI:Test/1234) Mode: Standard

Figure 4. Screen-shot of the Power Insight Configurator, Switching Configuration tab

If the Configurator reports that the gate drive is not recognised, then it is possible that the CPLD is a newer version than supported by the tool. In this case make sure the latest version is installed and if there is still a problem the Configurator database can be updated with a new file from the Amantys website. Refer to the User Guide supplied with the Power Insight Configurator for further details.

All configurable parameters on the gate drive can be set by selecting the Switching Configuration tab as shown in Figure 4.

Configurable parameters in this document are presented for ease of identification as follows:

| Parameter Name |
|----------------|
|----------------|



## 3 Gate Drive Overview

The gate drive contains the features shown in the block diagram, Figure 5.

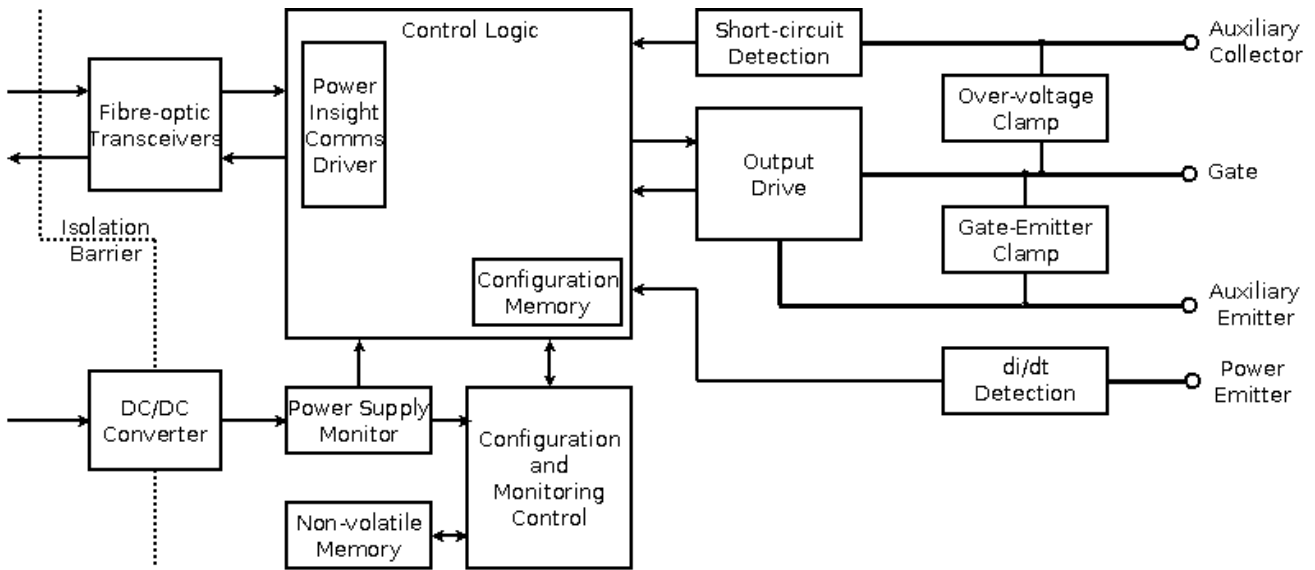


Figure 5. Gate Drive Block Diagram

### 3.1 Connecting to an IGBT

It is preferable if the gate drive can be located as close as possible to the gate and emitter connections of the IGBT module to minimise stray inductance and maximise control of the IGBT. The Module interface card (MIC) is mounted directly on the IGBT using the screw terminals provided.

To connect the gate drive to an IGBT, first mount the Module Interface Card (MIC) on to the IGBT using the screw terminals and cable terminations provided. Then connect the cable assembly to the gate drive, making sure there is no violation of creepage and clearance requirements. The gate drive, can then be located in an appropriate place in the converter.

It is recommended to use screws with internal spring shake-proof washers to connect the MIC to the IGBT module. This prevents loose washers from finding their way into the power assembly. Alternatively a combination of plain and spring washers are acceptable. In some cases washers may be required underneath the MIC to ensure there is sufficient mechanical clearance between the IGBT module and any components on the underside of the MIC.

Note: Carefully review the IGBT module mounting points to avoid interference with the components on the underside of the MIC. Do not over-tighten screws, and use the torque setting recommended by the IGBT module vendor.

### 3.2 Power Supply

The power supply input has a wide voltage range from 14V to 30V, although 15V or 24V is typical. Refer to datasheet for typical current consumption. The quiescent power dissipation is about 1.65W and the total power required is proportional to the switching frequency and IGBT gate charge.

The total power dissipation should be less than the value in the datasheet and can be calculated as follows,

$$P = 1.65 + Q_G \cdot f_{sw} \cdot \Delta V_{gg}$$

Where, P = power,  $Q_G$  = gate charge (from the IGBT datasheet),  $f_{sw}$  = switching frequency and  $\Delta V_{gg}$  is the gate voltage swing, typically 25V (i.e. from -10V to 15V).

### 3.3 Fibre-optic transceivers

Firecomms transceivers are used to implement the fibre-optic interface.

The Firecomms transmitter is an FT10MHLR and the receiver an FR50MHIR. Refer to Firecomms documents for details and interfacing information [\[1\]](#).

### 3.4 Measurement

The DC link voltage, i.e. the voltage across the IGBT when off and turning on, can be measured up to the voltage rating of the IGBT. Comparators with programmable references can be used for desaturation detection during turn-on.

To sense  $di/dt$  or current, the voltage across the emitter stray inductance may be measured. This requires a connection to the power emitter as well as the auxiliary emitter.

### 3.5 Immunity to high $dv/dt$ and $di/dt$

High  $dv/dt$  when an IGBT switches will cause a current to flow between the primary and secondary of the isolating transformer. To minimise this, the transformer capacitance is very low. High  $dv/dt$  can also cause coupling by capacitance into high value resistors (M $\Omega$ ). By careful layout of the on-module gate drive PCBs such resistors are shielded from nearby busbars, and we use digital filters on any signals that monitor the resistor chains. This is not so much of an issue for the AD33AA8P11 (AD00XA8) gate drive which is off module and can be located away from sources of  $dv/dt$ .

Regarding  $di/dt$ , there is always the chance of magnetic coupling into any loops of wire on or off the gate drive boards. The only solution is to keep the loop area as small as possible, either by routing tracks close together or close to a ground plane on the board. Digital noise filters are used to remove signals generated by short pulses of magnetic energy coupled into the gate drive circuits, such as  $di/dt$  comparators.

### 3.6 EMC compliance

Amantys gate drives are tested against railway and industrial motor drive standards for immunity and to ensure they are not a significant source of radiated emissions. By far the most significant source of emissions is when the IGBT itself switches. This can cause radiated emissions from any cables that exit the gate drive boards, the most significant of which is usually the power supply cable.

The railways standards require that the converter is tested for EMC compliance, but it is not always necessary to test at gate drive on its own. Emissions from the gate drive and cables will often be contained within the converter enclosure. In order to pass emissions tests on a gate drive that is outside of a converter, some measures are taken (such as an external common-mode choke) to limit the level of emissions. Please refer to the EMC test reports for further details.

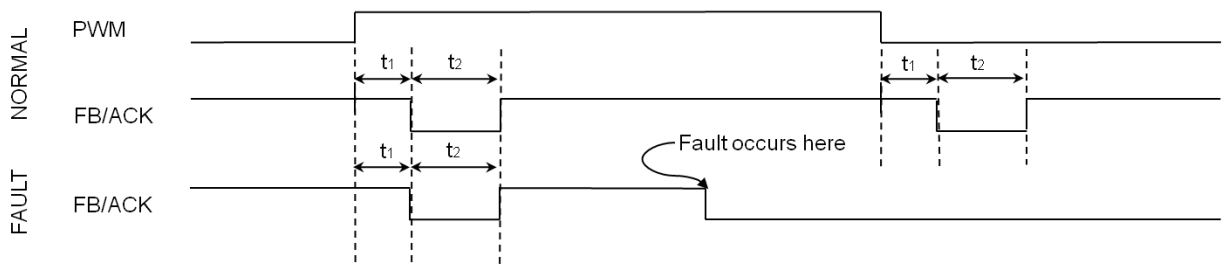
## 4 Fibre-optic Interface

### 4.1 PWM input

The gate drive responds to the edges of the PWM input signal. A rising edge (light off to on) will turn the IGBT ON, and a falling edge (light on to off) will turn the IGBT OFF.

### 4.2 Feedback Signalling (Amantys protocol)

When a change in the PWM input is received, an acknowledge signal is sent via the FB/ACK output as shown below. The FB/ACK output pulses LOW to indicate a PWM edge has been received. In the event of a fault the FB/ACK output goes LOW until the fault has been cleared. This scheme is compatible with many industry-standard plug and play gate drives.



**Figure 6. Feedback Protocol Timing Diagram**

| Parameter | Description                        | Units | Min | Typ | Max  |
|-----------|------------------------------------|-------|-----|-----|------|
| $t_1$     | PWM to FB/ACK (Compatibility Mode) | ns    | -   | 450 | 500  |
| $t_1$     | PWM to FB/ACK (Normal Mode)        | ns    | -   | 900 | 1000 |
| $t_2$     | FB/ACK pulse width                 | ns    | 500 | -   | 1000 |

Note: Measurements are made on the pins of the fibre-optic transceivers and do not take into account pulse distortion and delays due to the fibre-optic transceivers.

**Table 1. Feedback Protocol Timing Parameters**

Specific timing of pulses and pulse widths vary due to pulse width distortion and delays imposed by the fibre-optic transceivers. If the FB/ACK pulse is observed on an oscilloscope after power cycling it will be seen to vary in width as data is transmitted, this is known as Power Insight Compatibility Mode. If the gate drive is switched into Power Insight Normal Mode (or has been programmed to default to Normal Mode) then the width of the FB/ACK pulse will be the same for every switching edge. This is one way to tell which mode the gate drive is in and can be useful when developing communications infrastructure. Note also that the PWM to FB/ACK delay increases in Normal Mode. Further information about Power Insight can be found in 9.

## 4.3 Feedback Signalling (InPower equivalent protocol)

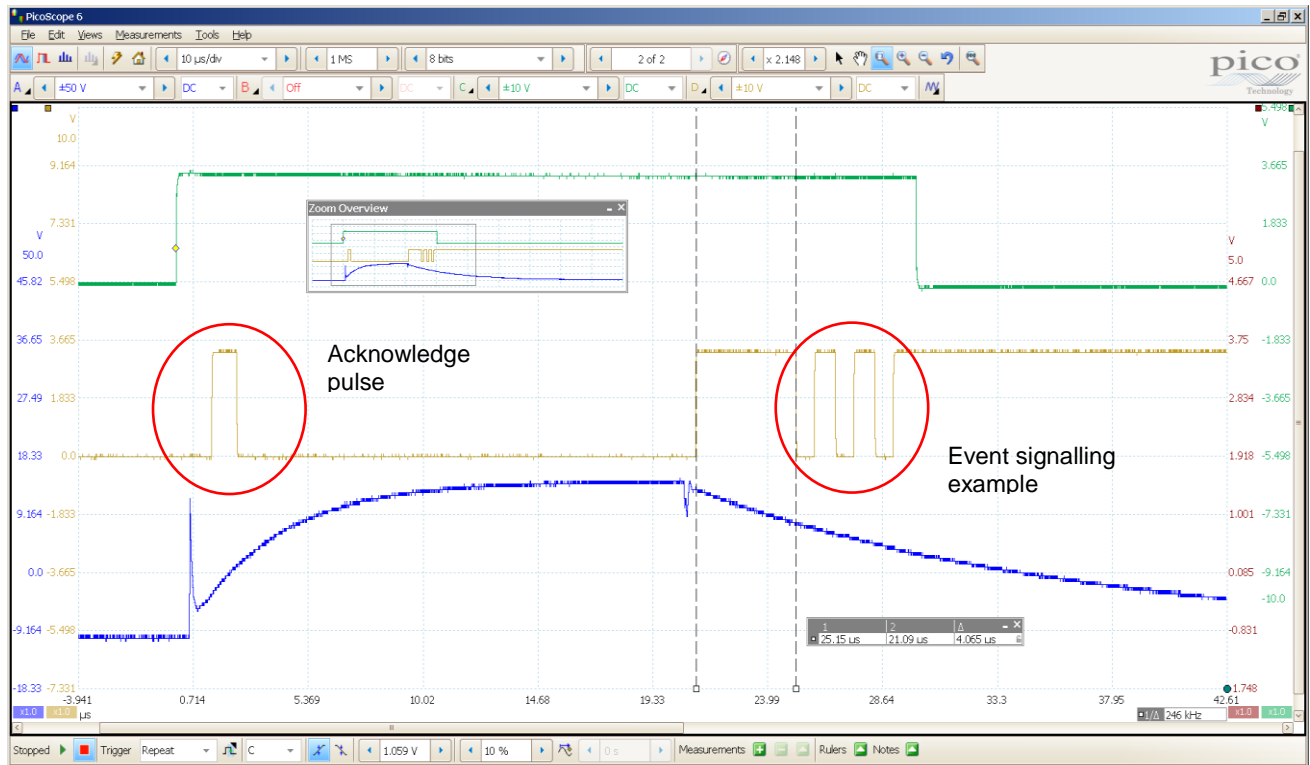


Figure 7. InPower Equivalent Feedback Protocol Timing Diagram

| Key |                   |
|-----|-------------------|
|     | PWM input         |
|     | FB/ACK (inverted) |
|     | Gate voltage      |

| Pulses | Event                | Pulse Measurement  |
|--------|----------------------|--|
| 1      | di/dt fault          | 0.75µs, 4µs after light goes off (logic high on diagram) |
| 2      | Short-circuit type 2 | 0.75µs wide, 0.80µs spacing                              |
| 3      | Not used             | 0.75µs wide, 0.80µs spacing                              |
| 4      | Not used             | 0.75µs wide, 0.80µs spacing                              |
| 5      | Short-circuit type 1 | 0.75µs wide, 0.80µs spacing                              |
| 6      | Narrow off pulse     | 0.75µs wide, 0.80µs spacing                              |
| 7      | Gate voltage fault   | 0.75µs wide, 0.80µs spacing                              |

Table 2. Feedback fault pulse meaning

## 4.4 Other Feedback Protocols

There are a number of other options for FB/ACK signalling, which have been designed to be compatible with OEM equipment. Programmable turn-on and turn-off delays can also be added to match existing gate drives and converter controllers. Please ask Amantys for advice if the default signalling is not suitable. The feedback protocol is set by the following parameter:

Feedback Protocol

The feedback protocol selected is defined in Table 3.

| Value | Protocol                          | Compatible with                  |
|-------|-----------------------------------|----------------------------------|
| 0     | Amantys Compatibility/Normal Mode | POWI, see Section 4.2            |
| 1     | Custom Mode 1                     | Refer to Amantys for information |
| 2     | Custom Mode 2                     | Refer to Amantys for information |
| 3     | Custom Mode 3                     | Refer to Amantys for information |
| 4     | Custom Mode 4                     | Refer to Amantys for information |
| 5     | Custom Mode 5                     | InPower, see Section 4.3         |
| 6     | Custom Mode 6                     | Refer to Amantys for information |
| 7..14 | Unused                            |                                  |
| 15    | Internal Signal                   | Used for debug purposes          |

**Table 3. Feedback protocols**

Custom Mode 5 (InPower equivalent) is described in 4.3, and details of the other custom feedback protocols are available on request from Amantys.

When the Feedback Protocol register is set to Internal Signal (value 15) an internal CPLD signal is routed to the FB/ACK output. The source of that signal is selected using the following parameter:

Debug

This is primarily for Amantys use and may be helpful for diagnosing faults in the field. The source of the FB/ACK signal depends on the gate drive configuration and may change, so Amantys will provide a value to program into this register if necessary.

In addition, there is a configuration parameter that is used during factory testing.

Test Config Enable

If this bit is set the red and green LEDs will blink together as a warning. Make sure this bit is set to 0 at all times.

#### 4.5 Fibre-optic drive current level

The following parameter can be used to set the fibre-optic transceiver drive current level. For longest life-time the current should be as low as possible allowing for the length of the optical fibre and for ageing of the transmitter. Values of around 3mA are recommended.

Fibre Drive Current

The range is 1.82mA to 6.37mA in 5 steps. At end-of-life it might be advantageous to increase the drive current, but this may also accelerate wear-out.

## 5 Drive Stage

The output drive stage is capable of sourcing and sinking current up to a maximum of approximately 30A, determined by the gate resistor settings and output MOSFETs. Gate-emitter capacitance can also be configured for compatibility with different IGBTs.

### 5.1 Turn-on and Turn-off Resistors

The turn-on resistance  $R_{G(on)}$  is selectable in the range  $0.47\Omega$  to  $27.0\Omega$  (63 values).

The turn-off resistance  $R_{G(off)}$  is selectable in the range  $1.02\Omega$  to  $56.0\Omega$  (63 values).

The soft-turn-off resistance  $R_{G(soft)}$  is selectable (63 values as for  $R_{G(off)}$ ), but is usually restricted to the range  $9.88\Omega$  to  $56.0\Omega$ .

These values are selected by setting the following parameters:

|                             |
|-----------------------------|
| Gate Turn On Resistor       |
| Gate Turn Off Resistor      |
| Gate Soft Turn Off Resistor |

During testing it is advisable to check power dissipation in these gate resistors which will depend upon the value set, the IGBT, and the switching frequency. A thermal camera can be used to check for hot spots. If the temperature of any gate resistor appears abnormally high then refer to Amantys for advice. It is possible that by choosing a different combination of resistors the hot spot can be eliminated.

Note: If an alternative set of resistors have been fitted to the gate drive, the real values of the resistors will be displayed in the Configurator.

### 5.2 Auxiliary Gate Capacitor

The auxiliary gate capacitance  $C_{GE(aux)}$  is selectable from 0nF to 328nF (16 values). The value is selected by setting the following parameter:

|                          |
|--------------------------|
| Gate-Emitter Capacitance |
|--------------------------|

Adding gate-emitter capacitance allows lower values of gate resistance to be used. This reduces switching time and controls  $di/dt$ , without significantly impacting  $dv/dt$ , therefore keeping switching losses down. Experimentation is required to find an optimal value. IGBT manufacturers sometimes recommend suitable values to get an acceptable trade-off between switching time, switching behaviour and low losses.

### 5.3 DC Link Measurement and High $V_{CE}$ Gate Turn-off Resistor

There is a  $V_{CE}$  comparator (Vce Monitor 4) that is used to select an alternative turn-off resistor for situations where the DC link is above a specific threshold. To avoid stress to the transient voltage suppressors (also known as TVS or transorbs) in the clamping circuit, it is desirable to slow down switching when the DC link is higher than usual for extended periods of time. For a full description of over-voltage clamping refer to 6.4.

Figure 8 shows the effect of increasing the turn-off resistor when the DC link is above a certain threshold, e.g. 2100V.

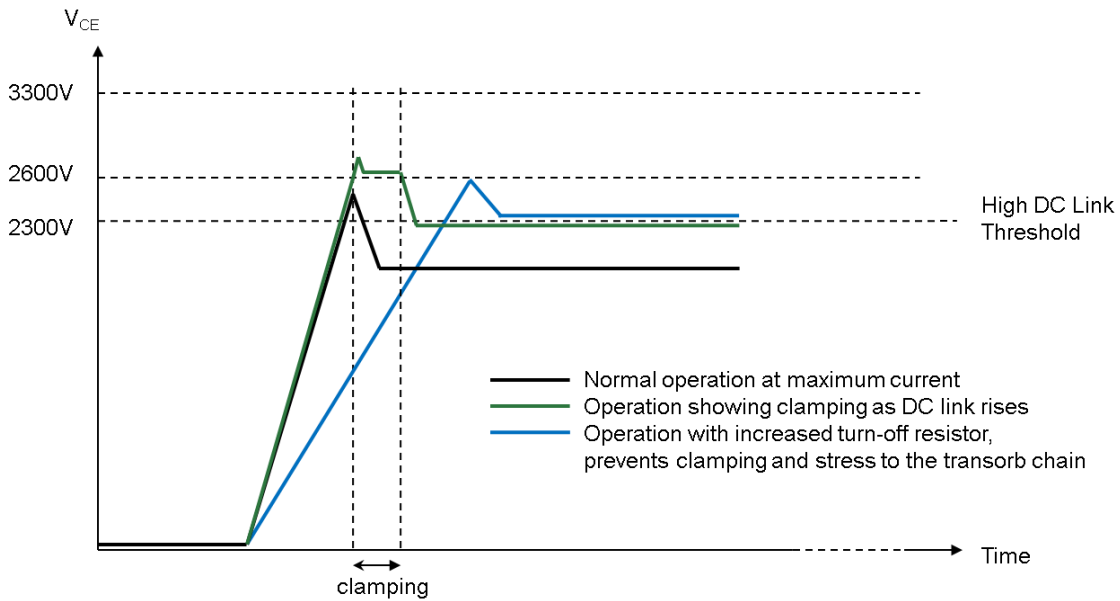


Figure 8. Effect of DC Link Measurement on turn-off switching waveform

To enable the feature, set the following parameters:

```
DC Link Measurement Enable
Vce Monitor 4 Comparator Threshold
High Vce Gate Turn Off Resistor
```

DC Link Measurement Enable is a single bit and the Vce Monitor 4 Comparator Threshold sets the high DC link threshold.

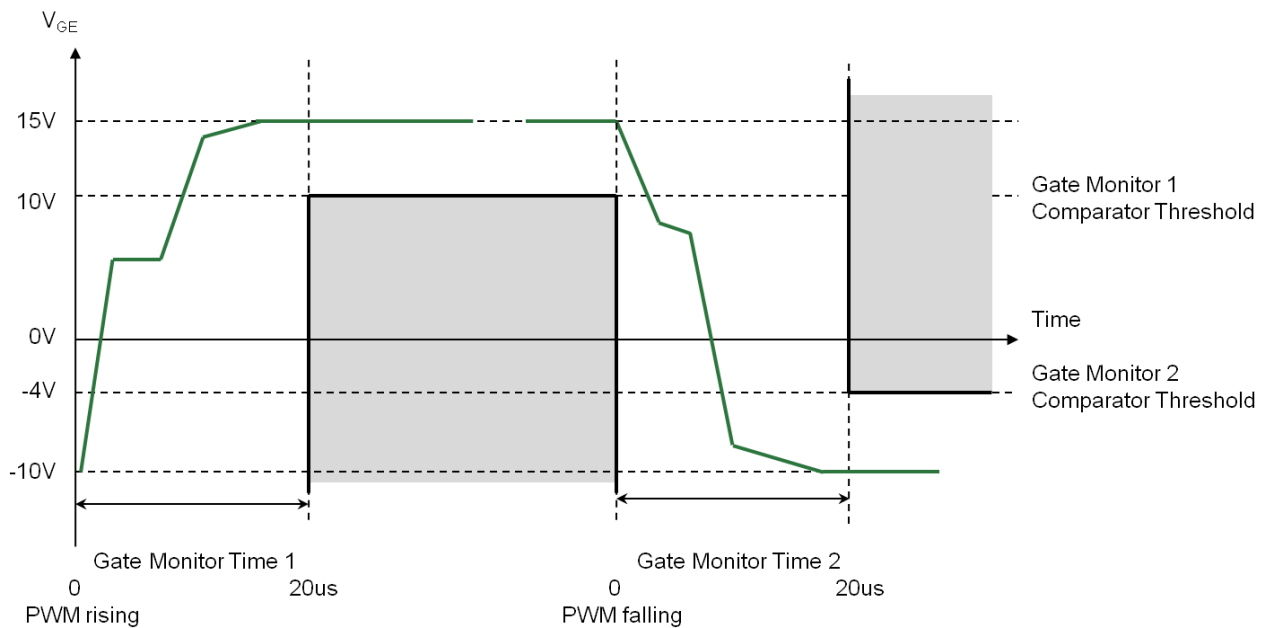
### 5.4 Gate Voltage Monitoring

It is possible to set voltage thresholds for the gate when on and off that generate a fault if not exceeded. The time at which the voltage is measured from the switching edge is also configurable. If the gate voltage does not exceed the threshold voltage, by the programmed time, the gate drive will generate a fault and turn-off. These measurements can be enabled or disabled using the following parameters:

```
Gate Monitor 1 Enable
Gate Monitor 2 Enable
Gate Monitor Time 1 (ON)
Gate Monitor Time 2 (OFF)
Gate Monitor 1 Comparator Threshold
Gate Monitor 2 Comparator Threshold
```

The Gate Monitor Enable parameters are single bits.

Figure 9, illustrates typical settings.



**Figure 9. Gate Voltage Monitoring with turn-on threshold at 10V and turn-off threshold at -4V, both at 20us**

## 5.5 Turn-on and Turn-off delays

It is possible to delay turn-on and turn-off to match the timing of other gate drives, or in the case of turn-on to add dead time. There are two parameters that control this behaviour which can be set in the range of 0 to 5µs as follows:

Turn On Delay  
Turn Off Delay

## 5.6 High Frequency Limiter

It is possible to limit the maximum frequency of operation to 4.4kHz for compatibility with existing converter controllers, and still allow double pulse testing with narrow pulses through the use of a frequency limiter. The limiter is enabled by setting the following parameter:

High Frequency Limit Enable

If this bit is not set then there is no restriction on the maximum frequency. However, at some point (depending upon the gate charge of the connected IGBT) the total power consumption will exceed the maximum available and the power supply will signal an under-voltage fault.

## 5.7 Short Pulse Detection

The minimum pulse width (or maximum frequency) can be defined and a fault will be generated if the pulse width is less than the time specified. The pulse width is defined as the time from one rising edge of the PWM input to the next rising edge of the PWM input.

To enable this protection, two parameters are defined:

Minimum Pulse Width  
Minimum Pulse Fault Enable



---

The pulse width can be from 0-1.3ms, although values of 50-100 $\mu$ s might be more appropriate. To enable the protection set the fault enable bit. Double pulse testing may be inhibited if this time is too long.

## 6 Protection Features

### 6.1 Gate-Emitter Clamp

The Gate-Emitter clamp connects the gate and emitter through a low impedance path when the gate drive is unpowered or if the programmable logic device is un-programmed. This holds the IGBT off and provides resilience to transients that could cause a spurious turn-on of the IGBT. This clamp is on the gate drive, so it will not protect the IGBT if the cable is disconnected.

### 6.2 Gate Drive Supply Under-voltage Protection

Under-voltage protection of the gate drive is provided to prevent operation of the IGBT at low input voltage and protect the IGBT module from damage due to high on-state losses resulting from low gate voltage. The gate drive contains under-voltage comparators to monitor the gate drive supply rails with respect to the 3.3V supply,

- Positive gate voltage:  $V_{g+}$ , e.g. for 15.0V the threshold is set at 12.5V
- Negative gate voltage:  $V_{g-}$ , e.g. for -10.0V the threshold is set at -6.5V

If any of the supplies drops below their thresholds the IGBT will be turned off and the FB/ACK output driven LOW to indicate a fault. The IGBT will remain off until the supplies are restored, the under-voltage timeout is exceeded and the PWM input is driven low to high.

The 3.3V supply is automatically monitored by the gate drive. If the supply falls below the minimum voltage threshold (2.375V) the outputs are turned off, which ensures the IGBT is held off.

There is a 45V supply for the desaturation protection circuits which is monitored (must be greater than 30V). Also the presence or absence of current ( $\sim 3\text{mA}$ ) flowing in the desaturation diodes is monitored by the gate drive. This protects against failure in the full desaturation protection circuit rather than just the supply voltage.

### 6.3 IGBT Short Circuit Protection

Short circuit protection of the IGBT is achieved by monitoring the IGBT for desaturation. The collector-emitter voltage ( $V_{CE}$ ) is monitored at switch-on and during the on state. If a short circuit (desaturation of the IGBT) is detected, the FB/ACK output is driven LOW to indicate a fault, and a type 1 or type 2 fault is recorded.

The conditions for the detection of the IGBT module desaturation are as follows. At switch on,  $V_{CE}$  is checked using various voltage comparators. If the  $V_{CE}$  voltage has not fallen below the monitored voltage in a specific time window then it is assumed that a short circuit or over-current event has occurred. If that event occurs within the first 10 $\mu\text{s}$  a type 1 event is recorded, and after that time a type 2 event is recorded.

A more thorough description of the desaturation protection and configuration registers can be found in Section 7.

On detecting a desaturation event the IGBT is turned off automatically by the gate driver and a fault signal indicated on the FB/ACK output. It is possible to prevent the gate drive turning off the IGBT (for use in 3-level converters) by setting the disable turn-off on fault configuration parameter:

Disable Turn-off on Fault

If disable turn-off on fault is set then the FB/ACK output immediately goes low (light off) to indicate a fault, and the converter controller must be designed to ensure that all IGBTs are turned off in the correct sequence before 10 $\mu$ s is exceeded.

After a fault has been detected, the IGBT gate will be held low (-10V) and switching will be inhibited for the duration programmed into the following parameter:

|                    |
|--------------------|
| Fault Lockout Time |
|--------------------|

This is to allow the IGBT chip temperature to stabilise and protect the IGBT.

To observe the flashing red LED it is suggested to set the Fault Lockout Time to 3 seconds during testing.

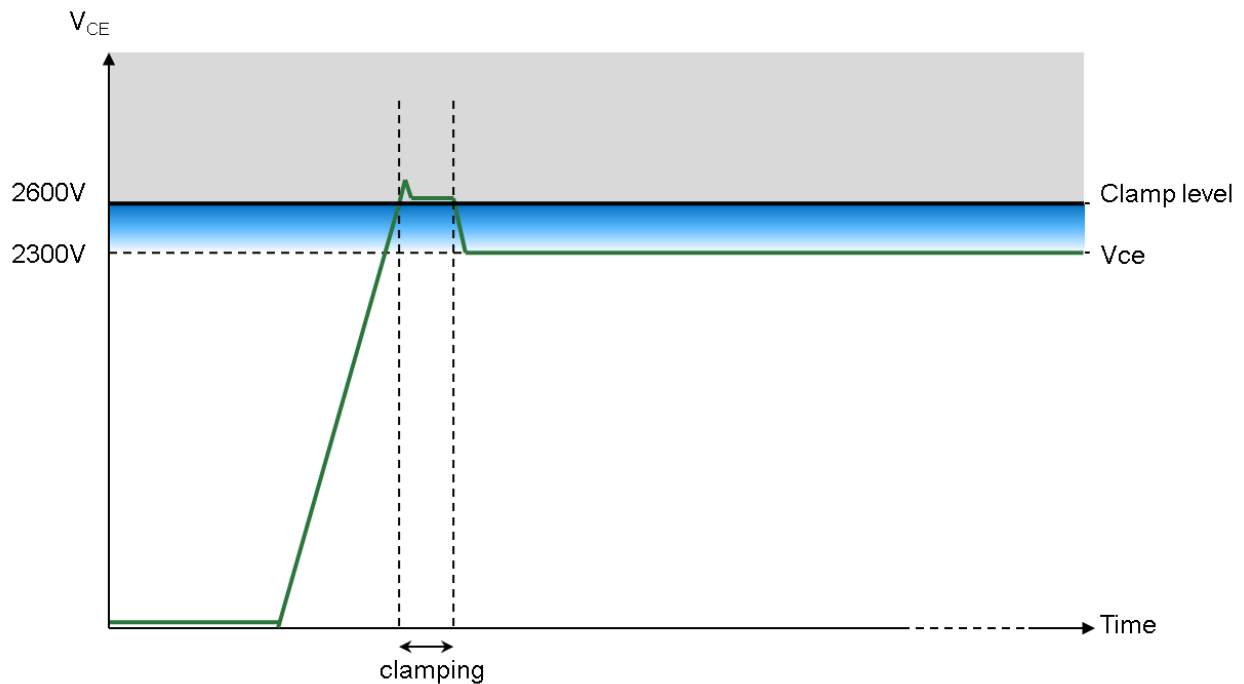
## 6.4 Over-voltage Clamping

At turn-off, when the IGBT is switching, the  $di/dt$  (the rate of change of collector current with respect to time) through the stray inductances in the power circuit may cause a transient voltage overshoot across the IGBT collector-emitter terminals. The overshoot can cause damage to the IGBT if it exceeds the IGBT maximum collector to emitter voltage rating,  $V_{CE(max)}$ .  $V_{CE}$  overshoots at turn off may be limited by the  $V_{CE}$  clamp. A discussion about clamping can be found in [2].

The clamp is implemented with a series string of transient voltage suppressors (also known as TVS diodes or transorbs) connected between the collector and the gate. As the collector voltage rises, the TVS chain conducts and current flows into the gate of the IGBT, effectively slowing down the turn-off.

Note: This gate drive does not implement two-level clamping which allows a higher DC link voltage to be used, whilst still clamping the turn-off overshoot.

A TVS is not a perfect component. It conducts over a range of voltage with conduction current increasing with voltage above the threshold. It also has a wide tolerance and temperature dependence. For this reason it is necessary to set the clamping level quite low compared to the maximum blocking voltage of the IGBT, for example 2300-2600V for a 3300V IGBT.



**Figure 10. Over-voltage Clamping**

The TVS components that implement the voltage clamping are mounted on the module interface card, which provides flexibility for use with different IGBT voltage ranges.

As mentioned earlier  $V_{CE}$  clamping works by temporarily increasing  $V_{GE}$  in order to soften the IGBT turn-off, keeping the IGBT in its active region for longer in order to control the  $di/dt$  slope and limit the overshoot voltage. When the energy in the stray inductance dissipates, the overshoot voltage decays and the IGBT turns off normally. This can be seen in Figure 11.

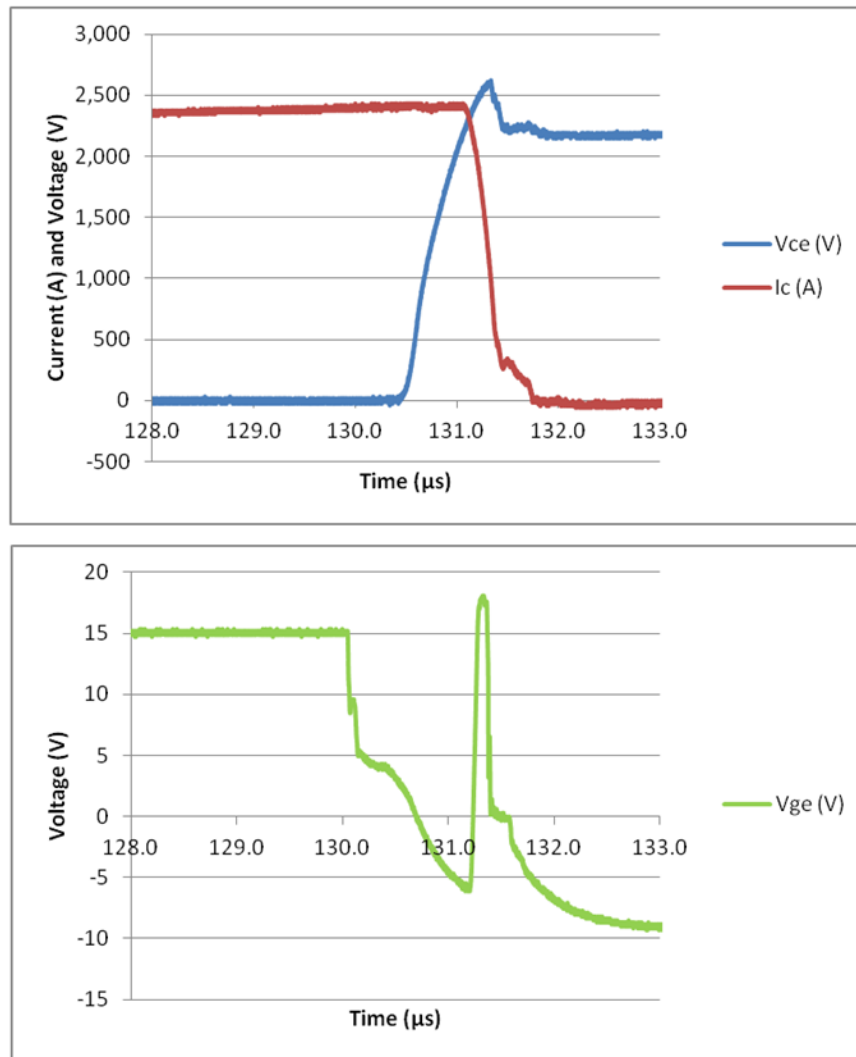


Figure 11. Over-voltage Clamping, showing gate voltage rise to slow down turn-off

## 7 Collector Voltage Monitoring and Desaturation Protection

The gate drive has both a potential divider and a current source with a chain of diodes for high voltage protection. In general, the current source is a more robust method of detecting short circuits because potential dividers implemented with very high value resistors (M $\Omega$ ), to limit power dissipation, can easily pick up interference.

The following sections describe the V<sub>CE</sub> monitors and diode desaturation protection. In general, the diode desaturation protection is preferred and the V<sub>CE</sub> monitors are only used for very slow switching IGBTs.

### 7.1 V<sub>CE</sub> monitors

There are three voltage comparators, used to measure V<sub>CE</sub>. These comparators are used to measure voltages above the desat diode chain maximum threshold of 36V. The voltage is set by configuring the following parameters:

```
Vce Monitor 1 Comparator Threshold  
Vce Monitor 2 Comparator Threshold  
Vce Monitor 3 Comparator Threshold
```

These can be enabled to operate in any of four time windows, as described below, using the following parameters:

```
Vce Monitor 1 Enable  
Vce Monitor 2 Enable  
Vce Monitor 3 Enable
```

Important: Each of these parameters is 4-bits wide (values 0-15) where bit 0 enables a monitor in time window 0, bit 1 enables a monitor in time window 1, and so on.

### 7.2 Desat diode chain

The desat diode chain enables a threshold to be set for detection of V<sub>CE(on)</sub> from 0 to 36V. There are two comparators.

```
Desat Diode 1 Comparator Threshold  
Desat Diode 2 Comparator Threshold
```

These can be enabled to operate in any one of four time windows, as described below, using the following parameter:

```
Desat Diode 1 Enable  
Desat Diode 2 Enable
```

Important: This parameter is 4-bits wide where bit 0 corresponds to time window 0, bit 1 to time window 1 and so on.

## 7.3 Configuring the desaturation protection

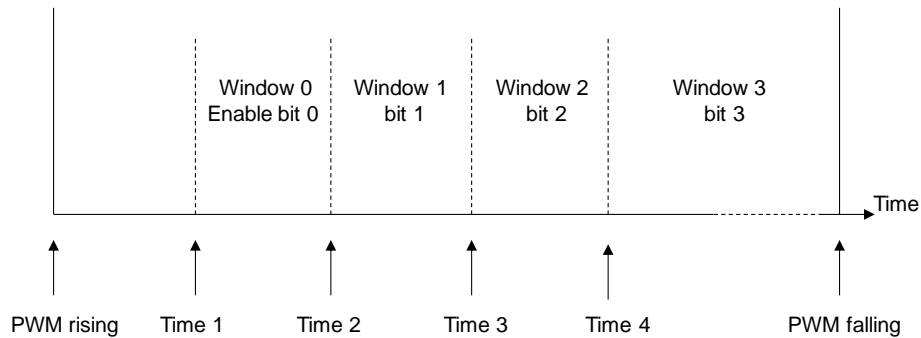
Four time parameters are provided to configure four time windows. They are:

Desat Window Time 1  
Desat Window Time 2  
Desat Window Time 3  
Desat Window Time 4

Each time is measured from the incoming PWM signal and is a value from 0 to 50µs. The physical timers can be programmed up to 1.31ms, but values above 50µs are not recommended as a fault may be generated. Time parameters can have the same value, but should adhere to the following relationship to correctly define the windows,

$$\text{Time 1} \leq \text{Time 2} \leq \text{Time 3} \leq \text{Time 4}$$

Figure 12, shows the relationship between time parameters, time windows and enable signals.



**Figure 12. Relationship between Time Parameters, Windows and Enable bits**

As an example for a very old IGBT, where  $V_{CE}$  falls slowly after turn-on, four windows and four voltage levels might be defined as shown in the diagram below, Figure 13.

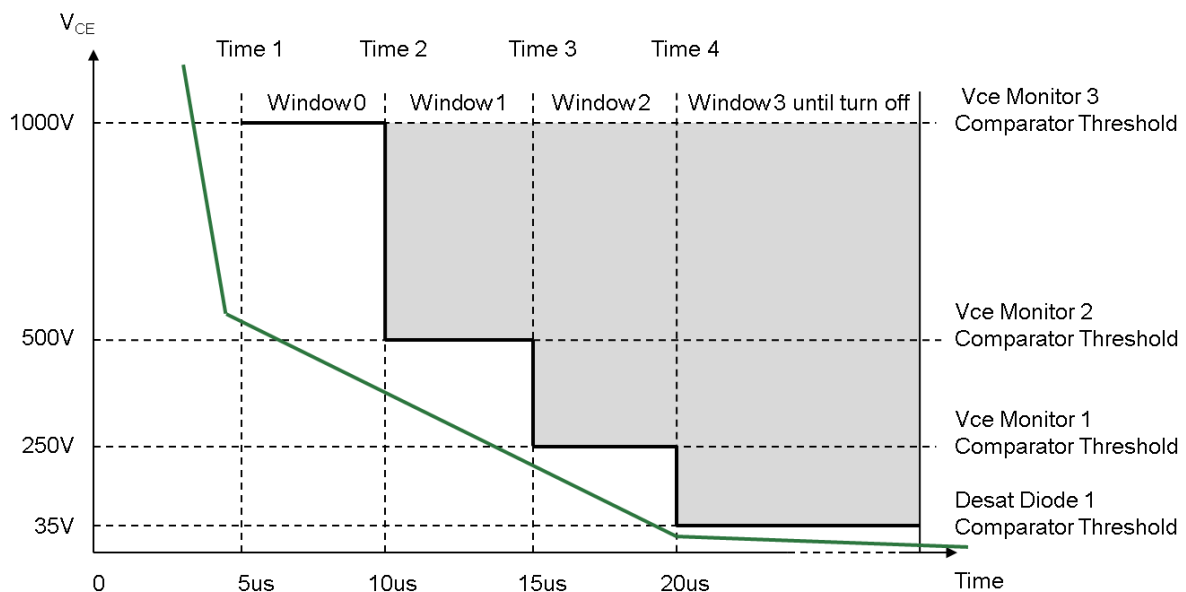


Figure 13. Desaturation Protection Example for Slow Switching IGBT; the green line is the collector voltage

The following tables describe the configuration parameter settings.

| Parameter            | Window |   |   |   | Value |
|----------------------|--------|---|---|---|-------|
|                      | 3      | 2 | 1 | 0 |       |
| Desat Enable 1       | 1      | 0 | 0 | 0 | 8     |
| Desat Enable 2       | 0      | 0 | 0 | 0 | 0     |
| Vce Monitor 1 Enable | x      | 1 | 0 | 0 | 4     |
| Vce Monitor 2 Enable | x      | x | 1 | 0 | 2     |
| Vce Monitor 3 Enable | x      | x | x | 1 | 1     |

Note: the bit order is reversed from what might be expected looking at the diagram, but defined this way so that it is easy to see the relationship between the bit position and the value programmed into the register.

x = don't care

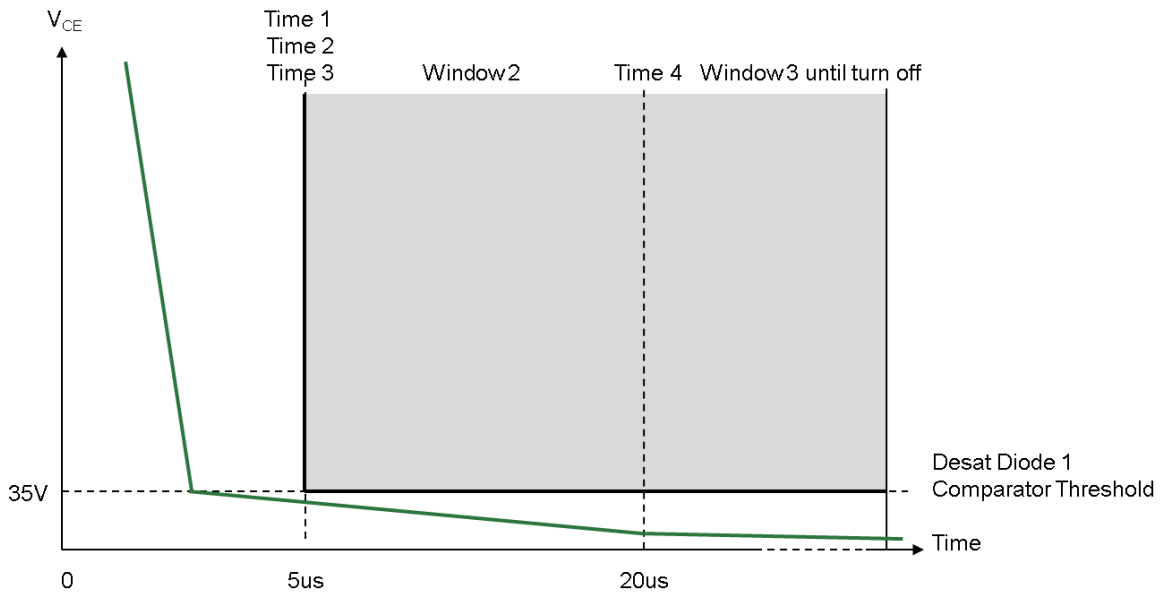
| Parameter                          | Value |
|------------------------------------|-------|
| Desat Diode 1 Comparator Threshold | 35V   |
| Desat Diode 2 Comparator Threshold | -     |
| Vce Monitor 1 Comparator Threshold | 250V  |
| Vce Monitor 2 Comparator Threshold | 500V  |
| Vce Monitor 3 Comparator Threshold | 1000V |

|                     |      |
|---------------------|------|
| Desat Window Time 1 | 5µs  |
| Desat Window Time 2 | 10µs |
| Desat Window Time 3 | 15µs |
| Desat Window Time 4 | 20µs |

Table 4. Example Parameters for Four Time Windows



Figure 14 is an example for a 3300V IGBT with just two windows and one voltage level.



**Figure 14. Desaturation Protection Example for 3300V IGBT; the green line is the collector voltage**

The following tables describe the configuration parameter settings.

| Parameter            | Window |   |   |   | Value |
|----------------------|--------|---|---|---|-------|
|                      | 3      | 2 | 1 | 0 |       |
| Desat Enable 1       | 1      | 1 | 0 | 0 | 12    |
| Desat Enable 2       | 0      | 0 | 0 | 0 | 0     |
| Vce Monitor 1 Enable | 0      | 0 | 0 | 0 | 0     |
| Vce Monitor 2 Enable | 0      | 0 | 0 | 0 | 0     |
| Vce Monitor 3 Enable | 0      | 0 | 0 | 0 | 0     |

Note: the bit order is reversed from what might be expected looking at the diagram, but defined this way so that it is easy to see the relationship between the bit position and the value programmed into the register.

x = don't care

| Parameter                          | Value    |
|------------------------------------|----------|
| Desat Diode 1 Comparator Threshold | 35V      |
| Desat Diode 1 Comparator Threshold | Not used |
| Vce Monitor 1 Comparator Threshold | -        |
| Vce Monitor 2 Comparator Threshold | -        |
| Vce Monitor 3 Comparator Threshold | -        |

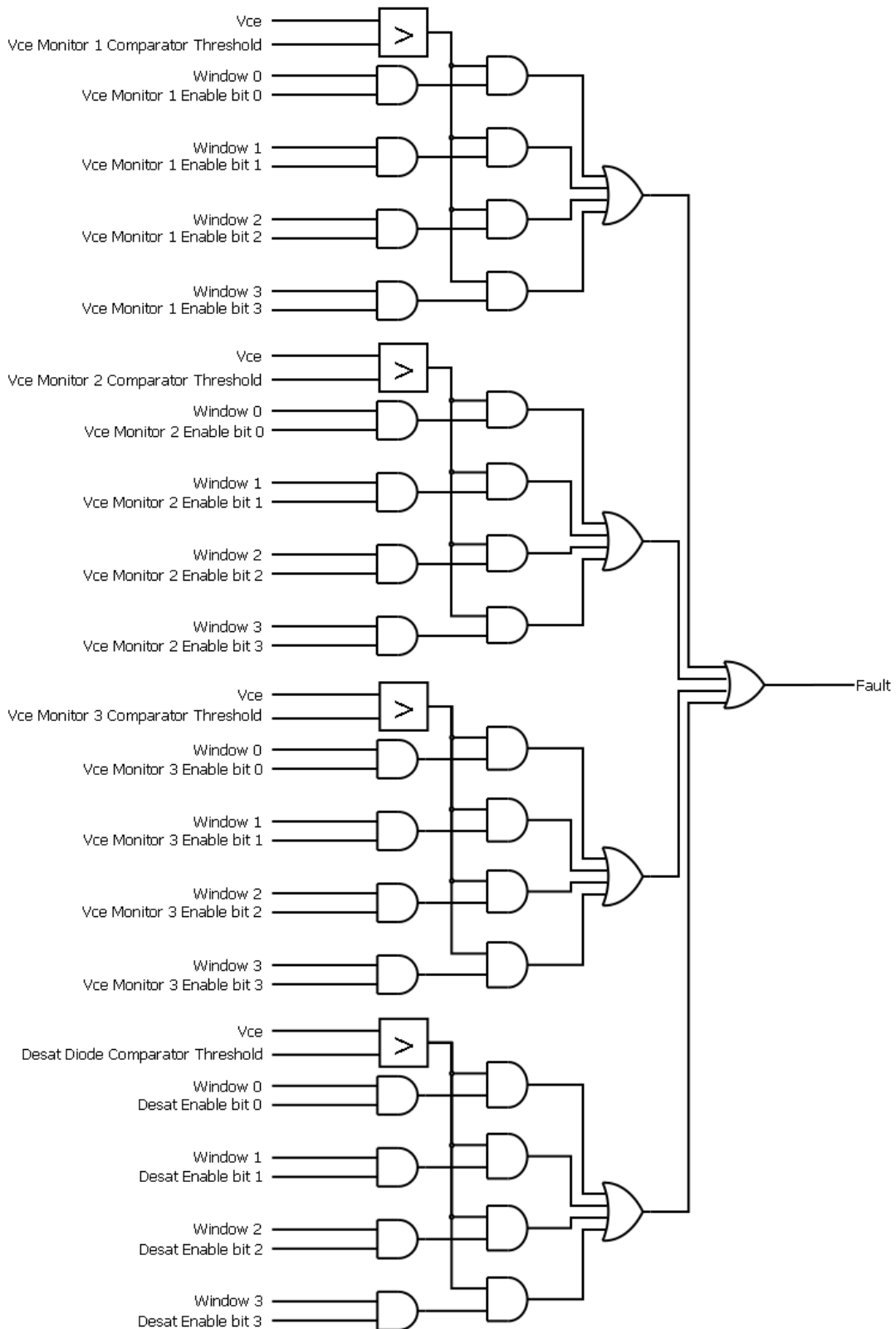
|                     |      |
|---------------------|------|
| Desat Window Time 1 | 5µs  |
| Desat Window Time 2 | 5µs  |
| Desat Window Time 3 | 5µs  |
| Desat Window Time 4 | 20µs |

**Table 5. Example Parameters for Two Time Windows**

Note the Desat Diode Comparator 2 Threshold is not used, but it could be set at a low value and used as an over-current detector in window 3 (i.e. after Time 4)

## 7.4 $V_{CE}$ Monitor and Desat Diode Filter

The various  $V_{CE}$  Monitor signals and the Desat Diode signal are combined with their respective enable bits and ORed together to form a single fault signal as shown in Figure 15.



**Figure 15. Fault Logic. Note: There are two Desat Diode comparators**

The fault signal is passed through a noise rejection filter with a time constant defined as follows. If the fault signal is high (logic '1') for more than the specified time constant then the gate drive will

signal a fault. The time constant for the filter can be configured in the range 0 to 5 $\mu$ s by setting the following parameter:

Vce Monitor Filter Time Constant

Note: For detection of short circuit type 1 (see 7.5), it is recommended that the sum of the filter time constant and the start of Time Window 1 should be less than or equal to 7.5 $\mu$ s. This means that in the event of a short, the fault signal will be asserted at 7.5  $\mu$ s after turn on, and with sufficient time to turn-off the IGBT within its 10 $\mu$ s rating (provided that the soft turn-off resistor  $R_{G(\text{soft})}$  is sufficiently low to turn off the IGBT within 2.5  $\mu$ s).

### 7.5 Type 1 and Type 2 short circuits

There are different definitions of type 1 and type 2 short circuits. Amantys defines a type 1 as a desaturation event within the first 10 $\mu$ s after the receipt of the incoming PWM turn-on command. Type 2 is any desaturation or over-current event after the initial 10 $\mu$ s. For a description of short circuit types refer to [3].

Typically type 1 short circuits occur when a device is switched on into a short, i.e. in the case of a shoot-through due to failure of the opposing IGBT in a phase leg or a direct short imposed from collector to emitter. Typical waveforms are shown in Figure 16.

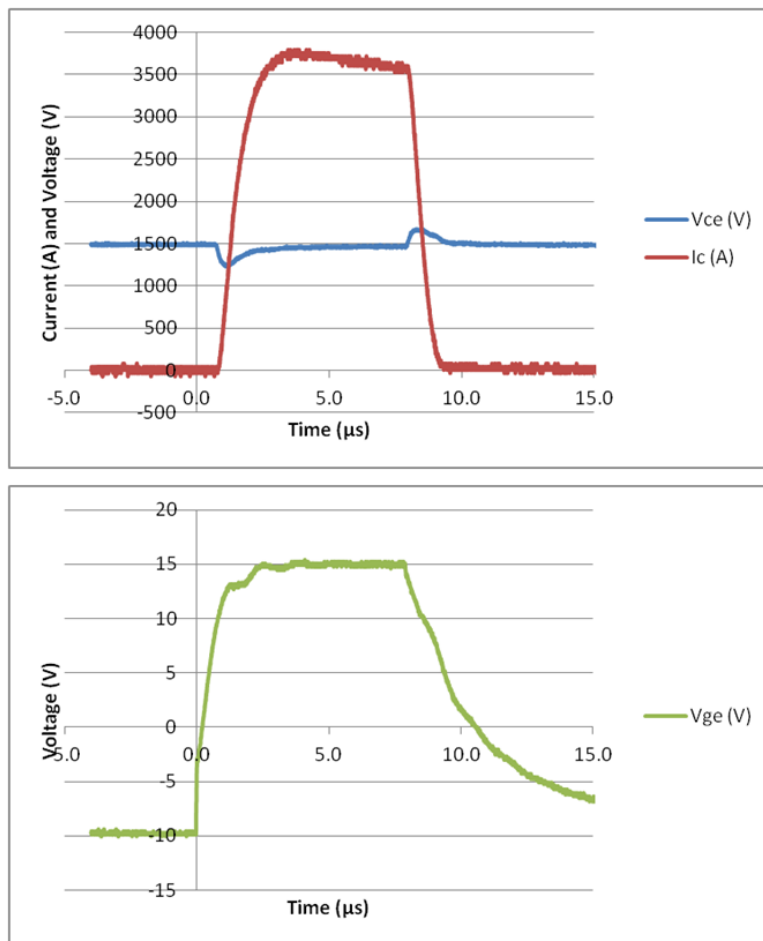


Figure 16. Short Circuit Type 1 showing turn-off before 10 $\mu$ s

Type 2 events generally occur due to a short in the load and are characterised by higher inductance and therefore slower current rise times. Typical waveforms are shown in Figure 17.

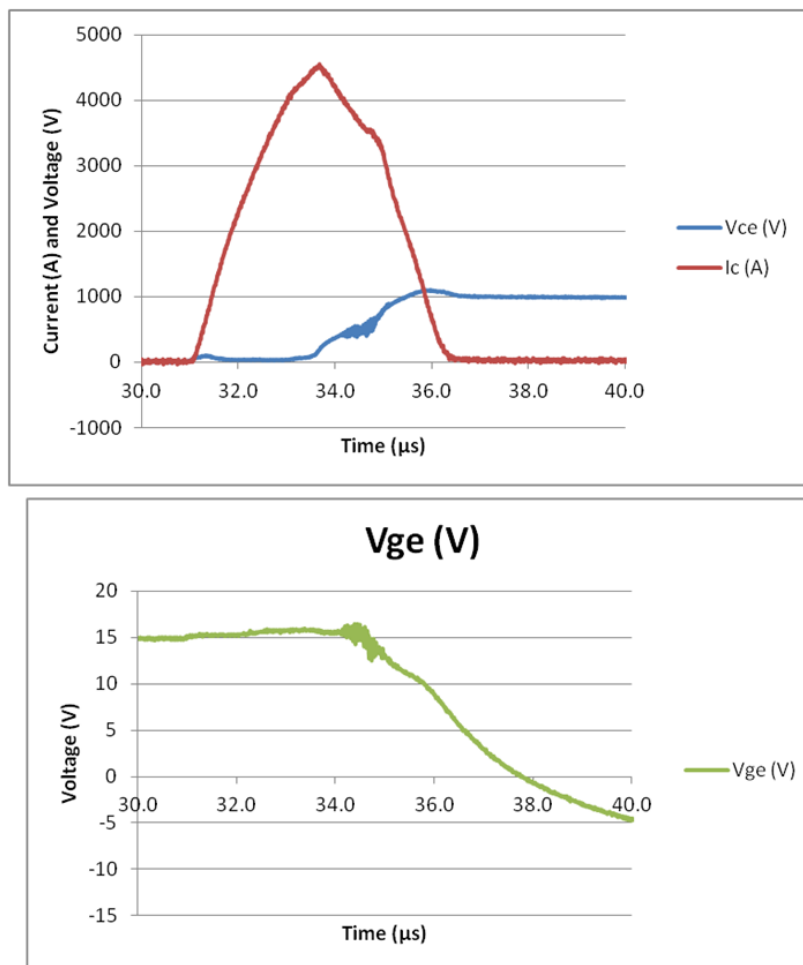


Figure 17. Short Circuit Type 2 detection and turn-off

Some IGBT manufacturers recommend that in the case of a type 2 short-circuit the current is allowed to stabilise before turning off. The following parameter allows this time to be set:

Type 2 Short Circuit to Turn Off Delay

This is a pure delay, which waits for a specific time from the fault signal going high before turning off the IGBT.

Note: It is unnecessary to set both a turn-off delay and a long Vce Filter Time Constant, see 7.4. So for example if the filter time constant is set at 3µs, then the IGBT will not be turned off until 3µs after the event is detected. It is recommended that the filter is used rather than this delay, unless there is a reason that a long filter time constant is not appropriate.

## 7.6 Inductive Type 2 short circuits

If the inductance of the short is large, then the  $di/dt$  during the short will be lower than in a hard short circuit. It is possible that the IGBT will be ON with higher than normal current for a long time. As the current is rising slowly, the IGBT may overheat before the device desaturates.

---

For this reason it is possible to set the Desat Diode 2 Threshold low, typically at least the value of  $V_{CE(on)}$  for twice rated current. Due to the existence of the high voltage blocking diodes in the diode desat detection circuit, it is necessary to add ~6V to the  $V_{CE}$  threshold read from the datasheet. Note also that this is temperature dependent, so a value in the range 15-20V may be sensible, but avoid values below 10V. To avoid false tripping please refer to Amantys for guidance.

Due to device margins there will always be a grey area between the maximum normal operating current, and the point at which desaturation or over-current is detected. Even with a circuit that measures  $di/dt$  it is difficult to set a comparator that can distinguish between normal and abnormal  $di/dt$ .

Amantys recommends that over-current detection is configured with knowledge of the application, circuit characteristics and possible fault scenarios.

## 8 di/dt Protection

Most Amantys gate drives do not implement di/dt protection for the following reasons.

To detect di/dt there needs to be a connection to the power-emitter of the IGBT module, which can be inconvenient. The voltage measured across the inductance between the auxiliary-emitter and the power-emitter is used to indicate the di/dt.

$$V = -L_s \cdot di/dt$$

Where  $L_s$  is the emitter stray inductance which is typically in the range of 5-10nH. If, for example, the di/dt to be detected is 2kA/ $\mu$ s and the inductance is 10nH then the voltage generated will be 20V. This is quite a low voltage level compared to the desaturation detection voltage which rises to 100's of volts very rapidly. For desaturation protection the diode desaturation protection mechanism is advised instead of di/dt protection.

Because there is a loop of wire between the auxiliary emitter and the power emitter this is also susceptible to pick-up inductively coupled noise. So, to use di/dt detection careful routing of cables is essential, and the system needs to be carefully configured to avoid false trips.

For compatibility with existing gate drives in the market, this gate drive has a dedicated power-emitter cable connection and does implement di/dt protection.

There are two configuration parameters defined to set two possible voltages:

```
di/dt Monitor 1 Threshold  
di/dt Monitor 2 Threshold
```

The threshold is a value from 0-255. Values less than 128 are negative voltages, corresponding to positive di/dt, and values above 128 are positive voltages corresponding to negative di/dt. Some experimentation is required to set up the levels. In general, the objective is to detect high di/dt that exists for a certain amount of time. To avoid tripping during a normal turn-on event there are two di/dt filters defined. Turn-on typically lasts for 500-2000ns, so it is advisable to set the di/dt filter time constant to a value greater than 2 $\mu$ s. Separate filters can be set of each of the thresholds.

```
di/dt Filter 1 Time Constant  
di/dt Filter 2 Time Constant
```

To enable the protection there are two bits defined, one for each of the thresholds and filters.

```
di/dt Enable 1  
di/dt Enable 2
```

The scaling of voltage levels to the 3V3 comparators used on the gate drive are set by resistors. These resistors can be modified for different scale factors but by default they are set so that the following mapping exists between the threshold value and the voltage detected.

---

If the di/dt Monitor Threshold = 0 this corresponds to a voltage of -15V. Therefore, if  $L_s = 10\text{nH}$ , then,

$$di/dt = -(-15\text{V} / 10\text{nH}) = 1.5\text{kA}/\mu\text{s}$$

If the di/dt Monitor Threshold = 255 this corresponds to a voltage of +15V. Therefore, if  $L_s = 10\text{nH}$ , then,

$$di/dt = -(15\text{V} / 10\text{nH}) = -1.5\text{kA}/\mu\text{s}$$

So the range is -15V to +15V with approximately 0.118V per bit.

To set up the di/dt protection use the following steps.

1. Decide which level of di/dt is a fault and calculate the di/dt Monitor 1 Threshold.
2. Decide for how long that level must be present for a fault to be indicated, and set the di/dt Filter 1 Time Constant.
3. Set di/dt Enable 1.
4. If more than one level and duration is required, repeat the process for monitor 2.

With this scheme positive and negative di/dt can be detected which may be useful in some circumstances.

If di/dt protection is not required, or there is no power emitter cable, leave the enable bits set to 0.

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## 9 Power Insight Communication

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Power Insight is a data communications mechanism that operates by superimposing a data signal onto the PWM and FB/ACK signals. It enables bi-directional communication between a converter controller and a gate drive using the existing fibre-optic interface. Power Insight defines two methods of sending data over the fibre-optic link: Compatibility Mode and Normal Mode. Compatibility Mode is so called because it is compatible with Power Integrations (CT-Concept) signalling.

### 9.1 Compatibility Mode

In Compatibility Mode the width of the acknowledge pulse is modulated to signal either a data '0' or '1'. This is uni-directional data transmission from gate drive to converter controller and is the default when the gate drive is turned on. The Power Insight adapter can be used to monitor the data, which comprises measurements and information about the gate drive. Because this is uni-directional it is not possible to change the data or send configuration information to the gate drive. For bi-directional communication the gate drive is switched into Normal Mode.

### 9.2 Normal Mode

A gate drive will switch from Compatibility Mode to Normal Mode whenever a data packet is sent which conforms to the Normal Mode protocol.

In Normal mode, pulses are modulated on to the fibre using a pulse-position modulation scheme to signal either a data '0' or '1'. This allows a much greater data rate (approximately 500kbits/s) compared to Compatibility Mode, and enables bi-directional communication.

When in Normal Mode a delay of 450-500ns is added to the PWM signal as it is received at the gate drive so that the data can be decoded from the PWM signal. The FB/ACK also incurs a similar delay as the data is encoded onto the line. A full system implementing bi-directional data communication will incur a total delay of <1us in each direction. For more information and assistance with Power Insight protocol, please contact Amantys.

### 9.3 Developing a Converter Controller that uses Power Insight

Amantys has developed the Power Insight Adapter and Power Insight Configurator to allow users to configure and monitor gate drives in the field during development and commissioning. To make use of the Power Insight features in a running converter it is necessary to develop a converter controller that is compatible with the Power Insight protocol. Typically this would involve integration of programmable logic for the physical interface and a processor to run the higher levels of messaging protocol. As every manufacturers' converter is different, the solution must be developed in conjunction with Amantys, so a discussion is recommended and it is worth considering the following questions,

- What measurements are required by the converter controller?
- How regularly are the measurements required, once an AC cycle or once a switching cycle?
- Are the measurements part of the converter's control or protection scheme?
- What is the interface between the converter controller and the Power Insight encoder/decoder?
- Is communication bi-directional, i.e. does the gate drive need to be updated regularly?



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## 10 Measurement of Voltage, Current and Temperature

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### 10.1 Analog-to-Digital Converters (ADC)

The microcontroller on the gate drive has an analog-to-digital converter (ADC) peripheral with multiple input channels. These are not used on this gate drive.

### 10.2 Event Counters

The gate drive contains a number of counters for counting events that have occurred since manufacture and since the last time the counter was reset. These are:

- Short Circuit Type 1 events
- Short Circuit Type 2 events
- Power Supply Under Voltage

By comparing the event counters on one gate drive with those on another in the same or similar stack, abnormal behaviour of a gate drive, IGBT or converter controller can be detected.

Note that in some cases a normal power-off event may be recorded as a power supply under-voltage as there is no way for the gate drive to detect the difference between a slow falling supply and a temporary under-voltage. Filtering has been applied to avoid recording multiple under-voltage events in quick succession; however this value is most useful when compared to the reading from other gate drives in the same converter.

### 10.3 On-board Temperature Sensor

A discrete temperature sensor or a temperature sensor in the micro-controller measures the gate drive temperature ( $T_{GD}$ ) and reports it by Power Insight in degrees Celsius. Due to local heating this reads approximately 15°C above ambient. As this is not an accurate measurement, it is best used relative to other gate drives in the converter as an indicator of abnormal conditions.

## 11 References

- [1] Firecomms data sheets [FR50MxxR Datasheet RevD.pdf](#) and [FT10MHLR Datasheet RevE.pdf](#).
- [2] See [littelfuse tvs diode protection for vfds igbt inverters.pdf](#) for a discussion about over-voltage clamping.
- [3] See [igbt-overcurrent-and-short-circuit-protection-in-industrial-motor-drives.html](#), for a discussion about short circuit types.

## Revision Table

| Revision | Comments  | Date        |
|----------|---|-------------|
| 01       | First external release based on P100191r07      | 20-Dec-2019 |
| 02       | Updated desaturation protection examples        | 13-Jan-2020 |
| 03       | Updated Table 2 on p12 with correct fault codes | 11-Feb-2020 |
|          |   |             |
|          |   |             |